REMARKS

Claims 1-20 are pending. By this amendment, claims 1 and 11 are amended. No new matter is introduced. Support for the amendments may be found at least on page 4, lines 6-11 of the specification. Reconsideration and allowance of all pending claims is respectfully requested in view of the preceding amendments and following remarks.

Claim Rejections Under 35 U.S.C. §102

Claims 1-20 are rejected under 35 U.S.C. §102 (b) over U.S. Patent 5,553,010 to Tanihira et al. (hereafter Tanihira). This rejection is respectfully traversed.

Tanihira is directed to a data shifting circuit capable of an original data width rotation and a double data width rotation. However, Tanihira does not disclose or suggest "each data input line has a one-to-one correlation to a single data transistor; ... all of the plurality of logic gates share a single data transistor for each data input" as recited in amended claim 1. There is no indication or suggestion that the logic gates of Tanihira, i.e., Logic I 110-113 & 15, Logic II 120-123 & 16, Logic III 130-133 & 17, and Logic IV 140-143 & 18, use a single data transistor for each data input, i.e., Din 0, Din 1, Din2, and Din 3.

The Examiner concedes on page 5 of the Office Action that Tanihira does not explicitly show a transistor receiving an input data. The Examiner asserts that "[i]t is known in the art that an AND gates are structured by transistors, and an input received by an AND gate as shown by Tanihira et al. must goes through a transistor as claimed." Applicants respectfully traverse. Prior art multiplexers and their disadvantages are described in the Background section of the present application at page 2, line 20 to page 3, line 5: "[m]ultiplexors are known in the art and use control signals to shift input data among output lines based upon the control signals. Multiplexors can require many inputs for the data lines and the control signals, and each data input can require a separate data line and individual transistor for interfacing the data line with a corresponding logic gate that performs the data shifting. Due to the high number of inputs, individual data lines increase the number of transistors required for each gate, thus increasing the area and power consumption of each gate."

The logic circuit for use in a multiplexer as recited in claim 1 solves the problem noted above and uses data sharing among transistors in order to reduces the number of transistors required by each logic gate. Referring to page, lines 12-16 of the specification, "instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines." For example, referring

to Figure 2A of the present application, a single data transistor 40 is required for data input DATL on logic gate 11. The data sharing on lines 61-64 provides for the elimination of additional transistors. "In particular, if logic gate 11 did not have data sharing, it would typically require an additional transistor for each of the data inputs on lines 61-64. Those transistors, if used, would interface the individual data lines with logic gate 11 in the same manner as transistor 40 interfacing data line 15 with logic gate 11. Elimination of those transistors results in a savings of area and power consumption." (See page 7, lines 9-14.)

Tanihira certainly does not disclose or suggest "each data input line has a one-to-one correlation to a single data transistor ... wherein all of the plurality of logic gates share a single data transistor for each data input" as recited in amended claim 1. Tanihira is directed to a barrel shifter with a plurality of data transistors per input data bit position. In other words, Tanihira's circuitry does not provide for data transistor sharing at all. For example, referring to Figure 6 of Tanihira, the four-to-one shifter requires 16 input data transistors for four output bit positions (with four logic gates). On the other hand, the logic circuit recited in claim 1 would only require four data transistors in a similar situation. Since Tanihira does not disclose or suggest all of the elements of claim 1, claim 1 is allowable over Tanihira.

Claims 2-10 are allowable because they depend from allowable claim 1 and for the additional features they recite.

Regarding claim 11, for at least the same reason as noted above with respect to claim 1, Tanihira does not disclose or suggest "each data input line has a one-to-one correlation to a single data transistor; ... all of the plurality of logic gates share a single data transistor for each data input" as recited in amended claim 11. Since Tanihira does not disclose or suggest all of the elements of amended claim 11, claim 11 is allowable over Tanihira.

Claims 12-20 are allowable because they depend from allowable claim 11 and for the additional features they recite. Withdrawal of the rejection of claims 1-20 under 35 U.S.C. §102 (b) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 8 and 18 are rejected under 35 U.S.C. §103 (a) over Tanihira in view of U.S. Patent 5,822,231 to Wong et al. (hereafter Wong). This rejection is respectfully traversed.

Claims 8 and 18 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 8 and 18 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above remarks, Applicant respectfully submits that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully Submitted,

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